The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte FRIEDRICH HAPKE

Appeal No. 2006-0943
Application No. 09/923,604

ON BRIEF

Before THOMAS, RUGGIERO, and BLANKENSHIP, Administrative Patent Judges.

BLANKENSHIP, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the examiner's final rejection of claims 1-3, which are all the claims in the application.

We reverse.

BACKGROUND

The invention relates to testing an integrated circuit, performing a test of the behavior of a combinational logic system in comparison with test software emulating the nominal behavior of the integrated circuit. Representative claim 1 is reproduced below.

> 1. An arrangement for testing an integrated circuit comprising a combinational logic system and a test circuit, which arrangement performs a test of the behavior of the combinational logic system in comparison with test software which emulates the nominal behavior of the integrated circuit, the arrangement comprising:
>
> two identical software models of the combinational logic system to be tested, in which a test sample is applied for test purposes to a first of these software models and whose output signals are coupled to a second of these software models;
>
> wherein the test circuit, in a test mode, applies a first test sample in a first test clock cycle to the input of the combinational logic system of the integrated circuit and receives the output signal in a buffer memory and which feeds back this output signal as a second test sample in a second test clock cycle to the input of the combinational logic system and again receives the output signal of the combinational logic system in the buffer memory
>
> wherein, at the end of the second test clock cycle, the arrangement compares the results of the combinational logic system of the integrated circuit in the buffer memory with the results of the second software model.

The examiner relies on the following references:

Kasuya	4,366,393	Dec. 28, 1982
Patel et al. (Patel)	5,377,197	Dec. 27, 1994

Ilker Hamzaoglu et al. (Hamzaoglu), Compact Two-Pattern Test Set Generation for Combinational and Full Scan Circuits, Int'l Test Conference Proceedings, pp. 944-53, Oct. 18-23, 1998.

Claims 1-3 stand rejected under 35 U.S.C. § 103 as being unpatentable over Kasuya, Patel, and Hamzaoglu.

We refer to the Final Rejection (mailed Apr. 4, 2005) and the Examiner's Answer (mailed Nov. 2, 2005) for a statement of the examiner's position and to the Brief (filed Sep. 6, 2005) and for appellant's position with respect to the claims which stand rejected.

OPINION

The statement of the rejection against claims 1 through 3 is set forth in the Office action mailed May 12, 2004. Appellant contests one of the examiner's findings with respect to Kasuya. According to the rejection, Kasuya discloses a test circuit, in a test mode, which feeds back an output signal to the input of a combinational logic circuit.

Appellant submits that Figure 4 of Kasuya illustrates the circuit in its test configuration, and demonstrates the lack of any feedback from the output of the logic circuit to the input of the logic circuit. (Brief at 7.) The examiner responds that logic circuit 100(100') in Figure 4 equates to the entirety of Figure 1, including the feedback circuit shown in Figure 1. Test circuit 100, illustrated in Figure 1, is the circuit applied against the claims. Test circuit 100, according to the examiner, includes the feedback that appellant contends to be missing. (Answer at 4.)

In view of Kasuya's description of Figures 1 and 4, and the inputs and outputs with respect to logic circuit 100(100') in Figure 4 as compared with the inputs and

outputs to circuit 100 in Figure 1, we consider the reference to support the examiner's position with respect to Figure 4. However, the reference does not support the examiner's position with respect to Figure 1.

Kasuya teaches that testing of an integrated logic circuit can be achieved by utilizing a different circuit structure from that of regular operation. The feedback loop of the sequential circuit is cut off from the combinational circuit. Random signals are used as test input, and the group of flip-flops are used to collect the test results. Col. 2, ll. 22-29. In the embodiment of Figure 1, multiplexer 4 supplies combinational logic circuit 1 with one of the random signal from random signal generator 3 and the output Y″ from register 2. Col. 3, ll. 18-28. In regular operation, register 2 operates as memory elements for the internal conditions of circuit 100. Multiplexer 4 supplies the output Y″ of register 2 as the feedback input Y′ of combinational circuit 1, effecting a sequential circuit. In the testing mode, however, multiplexer 4 supplies the random signal from random signal generator 3 to the combinational circuit 1. Col. 4, l. 44 - col. 5, l. 2.

Circuit 100 in test mode thus does not feed back the output signal to the input of the combinational logic circuit. Test mode results are stored in feedback shift register 2 (Fig. 3), which are obtained from line 110 (Fig. 1). The only feedback to combinational logic circuit 1, however, occurs during normal sequential circuit operation.

The provided evidence thus fails to support the examiner's findings in support of the rejection. A prima facie case for obviousness of the claimed subject matter has not been established. Cf. In re Zurko, 258 F.3d 1379, 1386, 59 USPQ2d 1693, 1697 (Fed.

Cir. 2001) (in a determination of unpatentability "the Board must point to some concrete evidence in the record in support of [the] findings."). We cannot sustain the rejection of claims 1 through 3 under 35 U.S.C. § 103 as being unpatentable over Kasuya, Patel, and Hamzaoglu.

CONCLUSION

The rejection of claims 1-3 under 35 U.S.C. § 103 is reversed.

REVERSED

JAMES D. THOMAS
Administrative Patent Judge

JOSEPH F. RUGGIERO
Administrative Patent Judge

HOWARD B. BLANKENSHIP
Administrative Patent Judge

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